45V / 350mA Low Drop-out Linear Regulator

Description

JLZ7375 is a high-performance low drop-out linear regulator with wide input voltage range at 3 ~ 45V and output current up to 350mA. The drop-out voltage is as low as 350mV at I_{OUT} = 100mA. The quiescent current is exceptionally small at 2.5μA. The device responds swiftly to transients over the output load and the line input.

PSRR performance of 73dB @ 1kHz makes the device a good fit for applications (e.g. 4G, WiFi module, smart wearables) in which clean supply line is often deemed critical. Armed with comprehensive protection features (thermal shut-down, short-circuit handling, current limiting) and precision band-gap reference, the device delivers accurate (± 2%) output voltages at 3.3V, 5.0V respectively. The device is manufactured [halogen, lead, antimony] free and RoHS compliant. Packages include: SOT-23-3L, SOT-23-5L, SOT-89-3L.

Features and Benefits

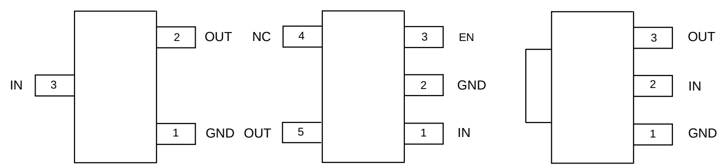
- Wide range of input voltages at 3 ~ 45V with maximum output current at 350mA
- Fixed output voltages with high accuracy (± 2%) at 3.3V, 5.0V
- Low quiescent current at 2.5μA
- Low drop-out voltage of 350mV at 100mA
- High noise rejection with PSRR of 73dB at 1kHz
- Excellent load regulation at 0.1 mV/mA and line regulation at 0.1 mV/V
- Built-in fault protection to minimize the effect of circuit hazards like short-circuit, over-current, and over-temperature
- Lead-free package assembled with ‘green’ molding compound

Applications

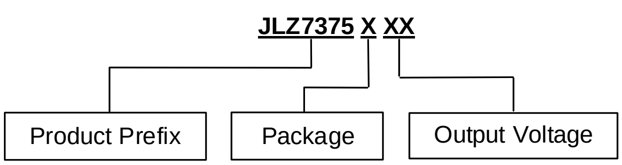
- Voltage regulation for wireless access modules
- Mainboards in Industrial robotics, remote networked clients, A/EIoT smart terminals
- Motherboards in telecommunication base station, power boards in commercial transportation and after-market add-ons

Pin Assignment

SOT-23-3L (Top View) **SOT-23-5L** (Top View) **SOT-89-3L** (Top View)



Ordering Information



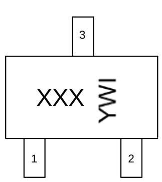
S: SOT-23-3L
S5: SOT-23-5L
Y: SOT-89-3L

33: 3.3V
50: 5.0V

Product Name	Package	Marking	MSL	T_J (ºC)	Media	Quantity (pcs)
JLZ7375S-33	SOT-23-3L	J733	3	-40 ~ 125	7" T&R	3,000
JLZ7375S-50		J750				
JLZ7375S5-33	SOT-23-5L	J733	3	-40 ~ 125	7" T&R	3,000
JLZ7375S5-50		J750				
JLZ7375Y-33	SOT-89-3L	J733	3	-40 ~ 125	7" T&R	1,000
JLZ7375Y-50		J750				

Marking Information

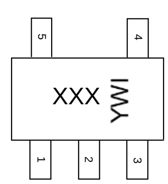
SOT-23-3L (Top View)



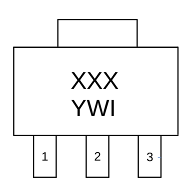
First Horizontal Line: Marking (see *Ordering Information*)

Second Line (Horizontal or Vertical): Date Code
Y: Year of Molding
W: Work-week of Molding
I: Internal Code

SOT-23-5L (Top View)



SOT-89-3L (Top View)



Typical Application Circuit

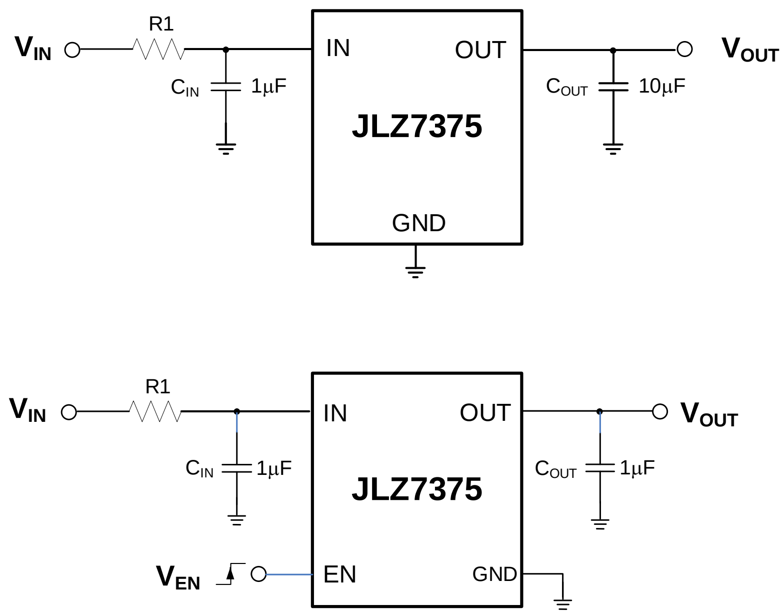


Fig. 1: Application Circuits

Functional Blocks

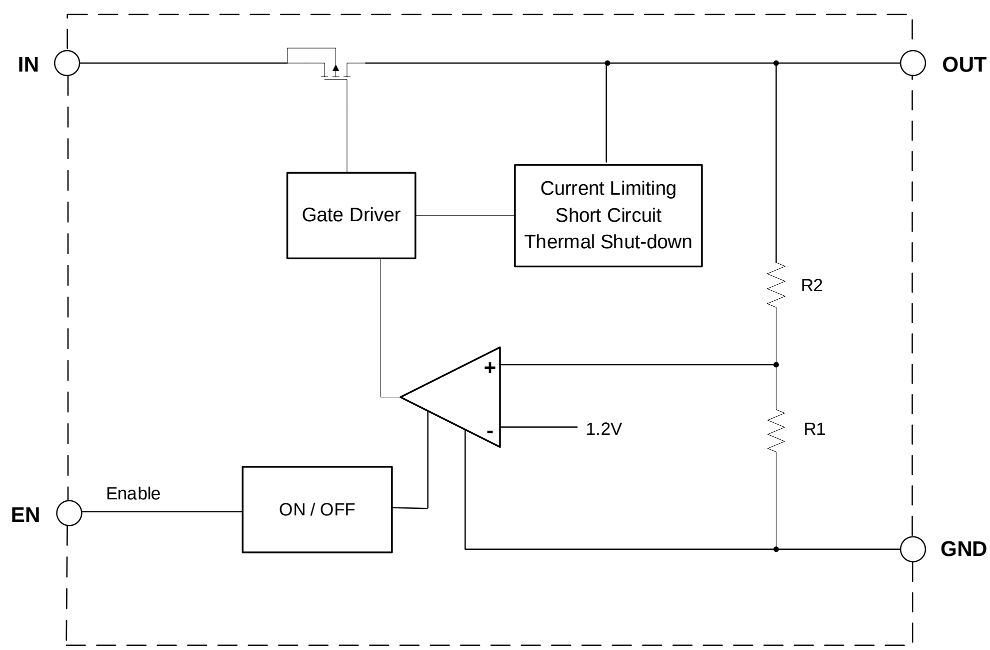


Fig. 2: Diagram of Internal Functional Blocks

Absolute Maximum Ratings [*1] (All measurements were made at T_A = 25°C unless otherwise stated)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OPER}	Operating Voltage Range	IN to GND	-0.3	55.0	V
		OUT to GND	-0.3	7.0	
		IN to OUT	-0.3	50.0	
		EN to GND	-0.3	55.0	
I_{OUT}	Output Current	Internally Limited	-	600	mA
T_J	Operating Junction Temperature	-	-	150	ºC
T_A	Operating Ambient Temperature	-	-40	125	ºC
T_{STG}	Storage Temperature	-	-40	150	
P_D	Power Dissipation	SOT-23-3L	-	600	mW
		SOT-23-5L	-	600	
		SOT-89-3L	-	900	
V_{ESD}	Human Body Model (HBM)	-	-	4	kV
	Charged Device Model (CDM)	-	-	200	V

Notes 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. While these are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” over extended periods may adversely affect the device reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IN}	Input Voltage	-	3	45	V
T_J	Operating Junction Temperature	-	-40	125	ºC

Electrical Characteristics

Test Conditions {V_{IN} = [V_{SET} + 1.0V]; C_{IN} = 1.0μF (ceramic); C_{OUT} = 10.0μF (ceramic); T_A = 25°C} are applicable to the following measurements unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage	-	3	-	45	V
I_{GND}	Quiescent Current	V_{IN} = 12V; no load	-	2.5	-	μA
I_{SHUT}	Shutdown Current	V_{IN} = 12V; EN = 0V	-	130	-	nA
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{OUT} = 10mA	V_{SET} * 0.98	V_{SET}	V_{SET} * 1.02	V
$I_{OUT-Max}$	Output Current	-	300	350	-	mA
V_{DROP}	Drop-out Voltage [*2]	I_{OUT} = 10mA; V_{IN} = V_{SET} - 0.1V	-	35	-	mV
		I_{OUT} = 100mA; V_{IN} = V_{SET} - 0.1V	-	350	-	mV
Reg_{Load}	Load Regulation, $\Delta V_{OUT} / \Delta I_{OUT}$	V_{IN} = 7V; 1mA ≤ I_{OUT} ≤ 100mA	-	0.1	-	mV/mA
Reg_{Line}	Line Regulation, $\Delta V_{OUT} / \Delta V_{IN}$	I_{OUT} = 1mA; [V_{SET} + 0.5V] ≤ V_{IN} ≤	-	0.1	-	mV/V
I_{LIMIT}	Current Limit Threshold	-	-	500	-	mA
PSRR	Power Supply Rejection Ratio	V_{IN} = 10V; I_{OUT} = 10mA; f = 1kHz V_{OUT} = 3.3V	-	73	-	dB
V_{ENH}	EN Input Voltage - Logic 'H'	Device turned ON	1	-	45	V
V_{ENL}	EN Input Voltage - Logic 'L'	Device turned OFF	-	-	0.4	V
T_{TSD}	Thermal Shut-down Threshold	Temperature rising	-	144	-	°C
		Temperature falling	-	126	-	°C

Notes 2: Dropout Voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.

Thermal Properties

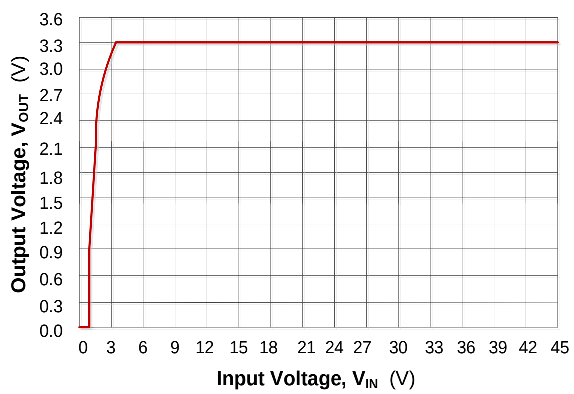
Test Conditions: Device mounted on FR-4 substrate, 2-layer PCB, 2oz copper, with minimum recommended cooling pad to dissipate heat

Symbol	Parameter	Conditions	Rating	Unit
$R_{\Theta JA}$	Thermal Resistance (junction-to-ambient)	SOT-23-3L	200	ºC/W
		SOT-23-5L	200	
		SOT-89-3L	130	

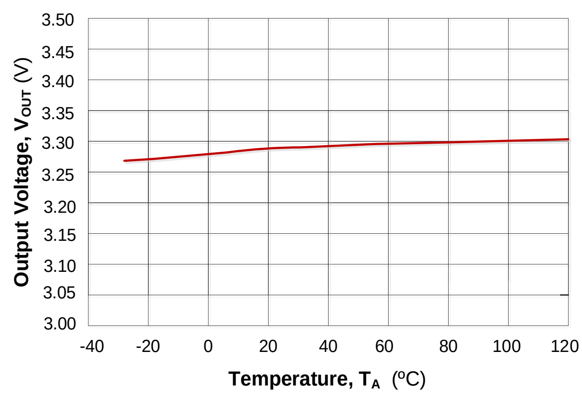
Typical Performance Characteristics

Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; I_{OUT} = 1mA; C_{OUT} = 10µF; T_A = 25°C

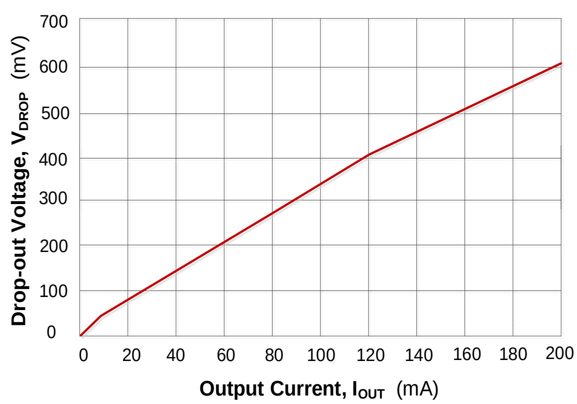
Graph 1: Output Voltage vs. Input Voltage



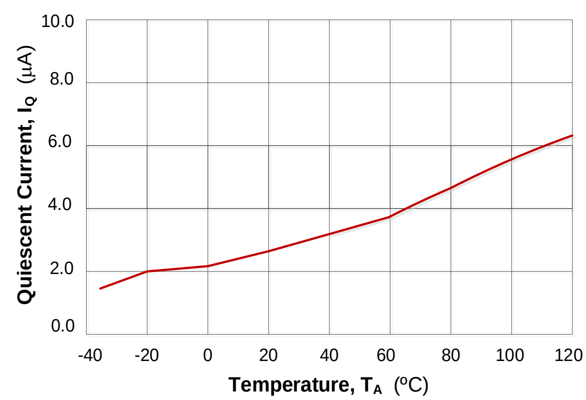
Graph 2: Output Voltage vs. Temperature



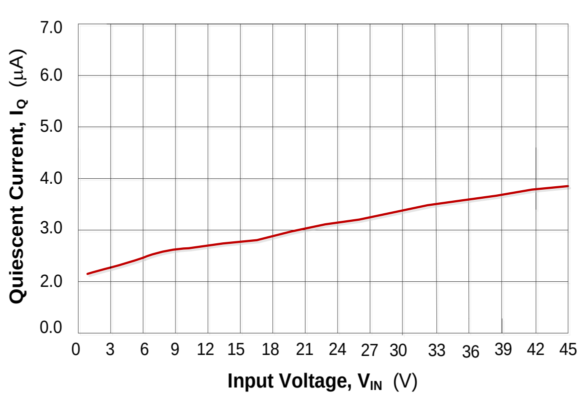
Graph 3: Drop-out Voltage vs. Output Current



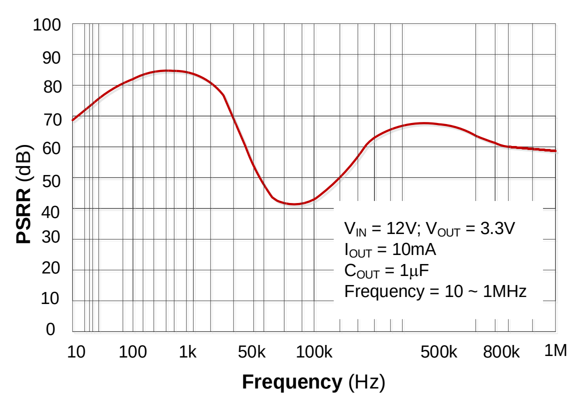
Graph 4: Quiescent Current vs. Temperature



Graph 5: Quiescent Current vs. Input Voltage



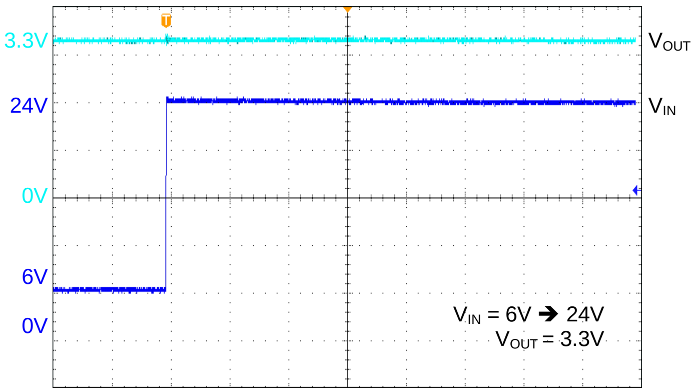
Graph 6: Power Supply Rejection Ratio vs. Frequency



Typical Performance Characteristics (Continued)

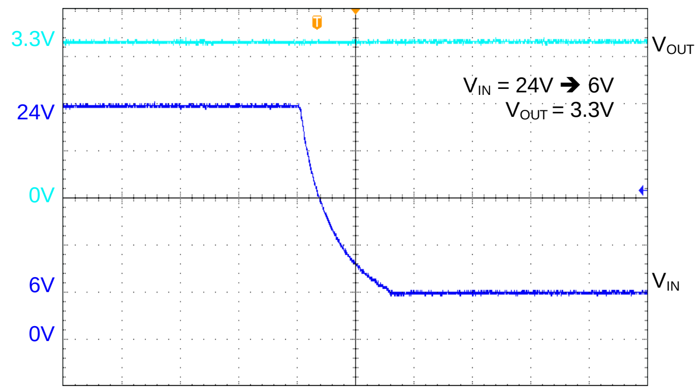
Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; I_{OUT} = 1mA; C_{OUT} = 10µF; T_A = 25°C

Graph 7: Response to Line Transients ↑



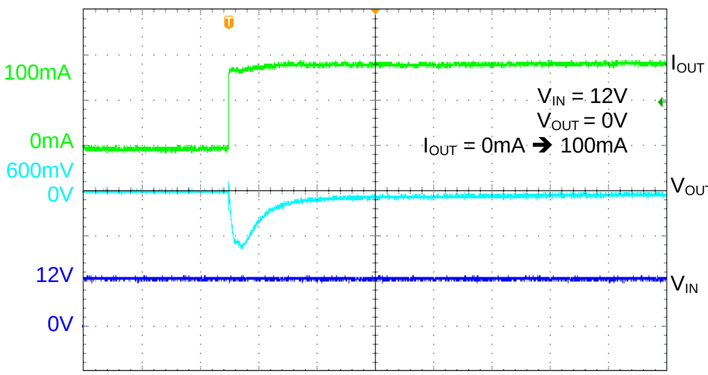
Time @ 4µs/div.

Graph 8: Response to Line Transients ↓



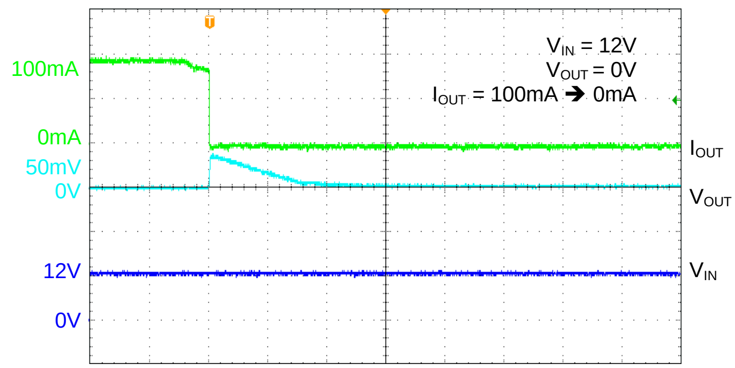
Time @ 4µs/div.

Graph 9: Response to Load Transients ↑



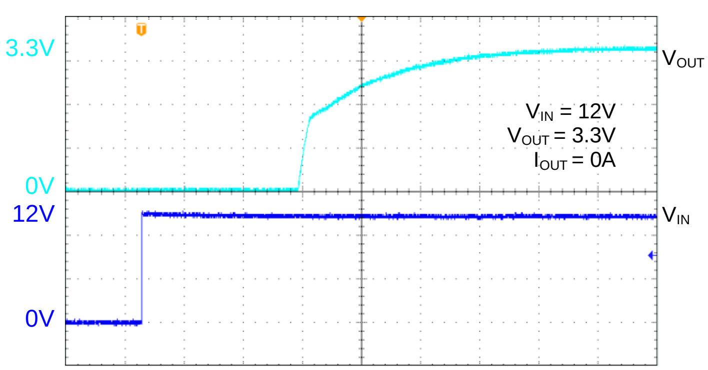
Time @ 200µs/div.

Graph 10: Response to Load Transients ↓



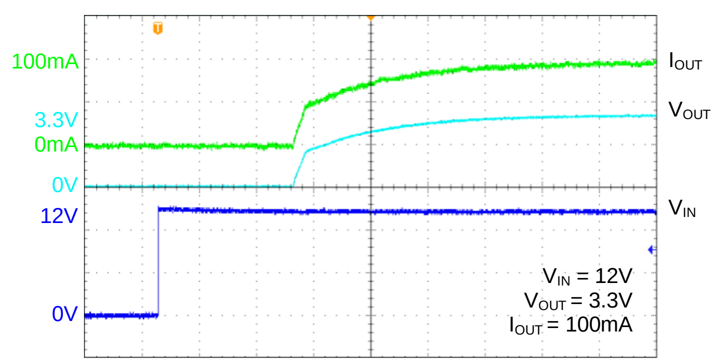
Time @ 200µs/div.

Graph 12: Start-up with no Load at OUT Pin



Time @ 40µs/div.

Graph 13: Start-up with I_{OUT} = 100mA at OUT Pin

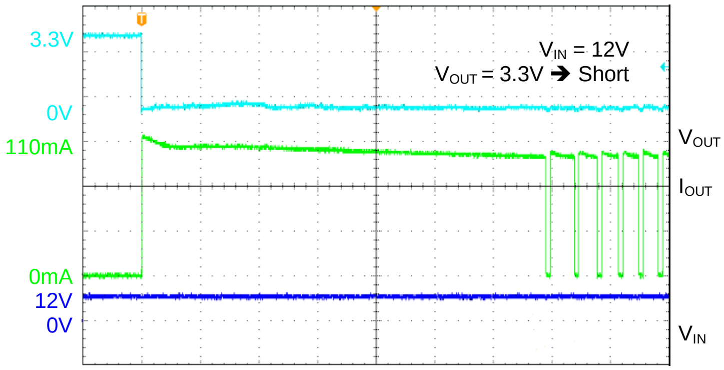


Time @ 40µs/div.

Typical Performance Characteristics (Continued)

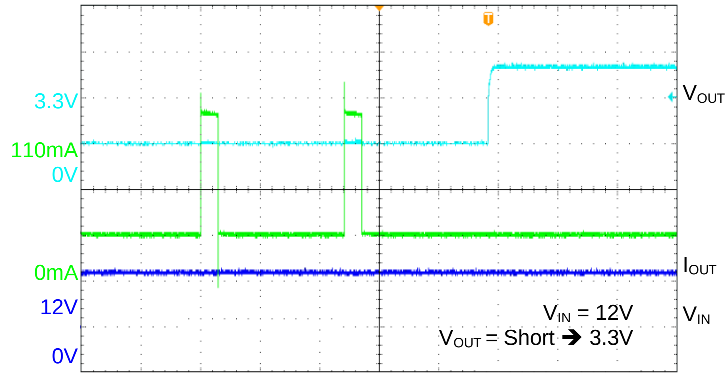
Unless otherwise stated, the following test conditions apply: V_{IN} = 12V; V_{OUT} = 3.3V; I_{OUT} = 1mA; C_{OUT} = 10µF; T_A = 25°C

Graph 14: Short-circuit Protection Assert



Time @ 2ms/div.

Graph 15: Short-circuit Protection Dis-asserted



Time @ 2ms/div.

Detailed Description of Device Operation

Overview

JLZ7375 is a power-efficient linear regulator with ultra-wide input voltage range from 3V to 45V and output current at up to 350mA. Three output voltage levels are offered: 3.3V, 5.0V.

The device offers low drop-out voltage at down to 55mV typically. The quiescent current is designed to be at a very low 2.5µA typically. The PSRR performance is an outstanding 73dB at frequency of 1kHz while both load and line regulation are highly accurate at ± 2% typically. In order to protect the device from operation hazards, full suite of fault detection & handling is embedded.

Input and Output

In order to de-couple the noise and glitch present on the power line at the input of JLZ7375 and the circuit board on which the device is populated, input capacitor (C_{IN} in Fig. 1) of ceramic type with value of 1µF shall be populated as close as possible to the IN pin. Wide copper trace is required between the IN and the GND pins. When $V_{IN} \geq 18V$, a resistor (R1) shall be added to the IN pin (c.r. Fig. 1) to protect the device from damage by in-rush. While the value of R_{IN} is dependent on the actual application in which the device is deployed, it must be larger than 1Ω.

In order to ensure loop stability and to improve the response of the device to load & line transients, output capacitor (C_{OUT} in Fig. 1) of ceramic type with value of at least 10µF shall be populated as close as possible to the OUT pin. The effective series resistance (ESR) of the output capacitor shall lie between 1mΩ and 5Ω.

Enable Feature

The device can be turned ON or OFF by driving the EN pin to either logic 'H' or logic 'L'. To ensure proper operation of the device, this pin must not be left unconnected. If the enable function is not used, this pin must be tied to the IN pin at all time such that the device remains at ON state all the time.

Current Protection

In the design of JLZ7375, fault detection & handling are in place to ensure device reliability and operation safety. These are the current limiting and short-circuit handling. Whenever one or multiple of the following conditions occur, the output current shall be clamped to a preset level (~ 100mA) to prevent damage to the load and the device from over-heat.

1) Output current at the OUT pin is higher than the current limit threshold (I_{LIMIT})
2) OUT pin is shorted to the GND pin

Thermal Protection & Power Dissipation

When the junction temperature (T_J) of the silicon die assembled inside the device goes up beyond the normality, due either to excessive loading or short-circuit at the OUT pin, the built-in thermal shut-down protection shall be triggered. The on-die power MOSFET shall be turned OFF to prevent the device from electrical overload. Once the abnormality disappears or the junction temperature of the die comes down, the device shall resume its standard operation.

As the device operates in its typical manner, the junction temperature of the internal die goes up inevitably. Ability of the package assembly (bonding wires, lead frame, die-attach material, epoxy, etc.) to dissipate the heat generated within shall determine the overall power dissipation, P_D:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}$$

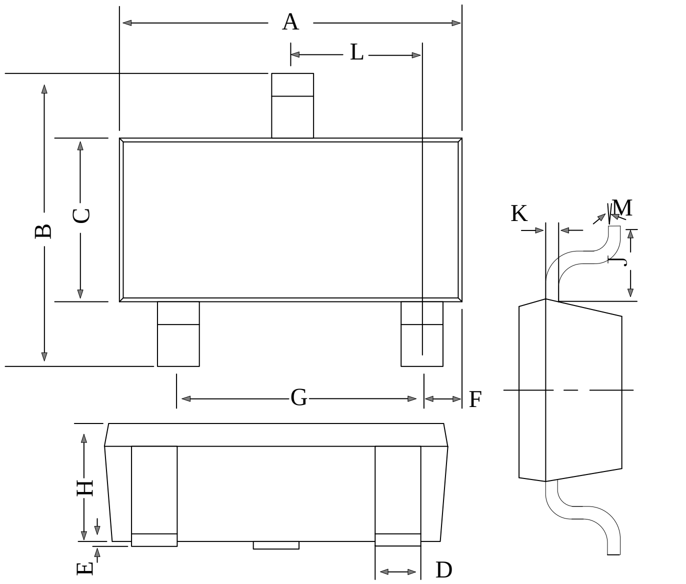
In reference to the junction-to-ambient thermal resistance ($R_{\Theta JA\_PCB}$) of the circuit board on which the device is populated, the junction temperature of the die inside the device's package can be estimated using the following equation:

$$T_J = T_A + P_D * R_{\Theta JA\_PCB}$$

The value of $R_{\Theta JA\_PCB}$ is determined, though not exclusively, by the following factors: power dissipation of the device, air flow and ambient temperature of the operating environment, PCB area, size & thickness of the copper thermal pad or the external heat sink (if any) attached, closeness of the components populated around the device, etc.

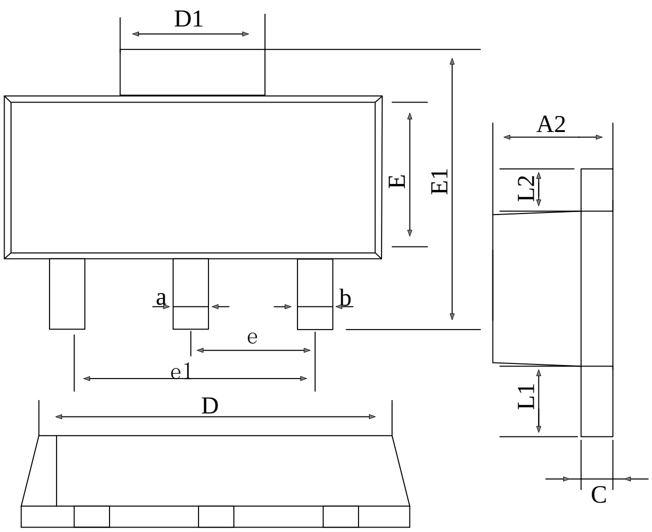
Package Outline (All measurements in mm)

Package Type: SOT-23-3L (J1)



SOT-23-3L (J1)		
Dimension	Min.	Max.
A	2.82	2.92
B	2.65	2.95
C	1.56	1.60
Dimension	0.35	0.55
E	0.00	0.10
F	0.45	0.55
G	1.90 RFF.	
H	1.00	1.30
K	0.10	0.20
J	0.40	-
L	0.85	1.15
M	0°	10°
All measurements in "mm"		

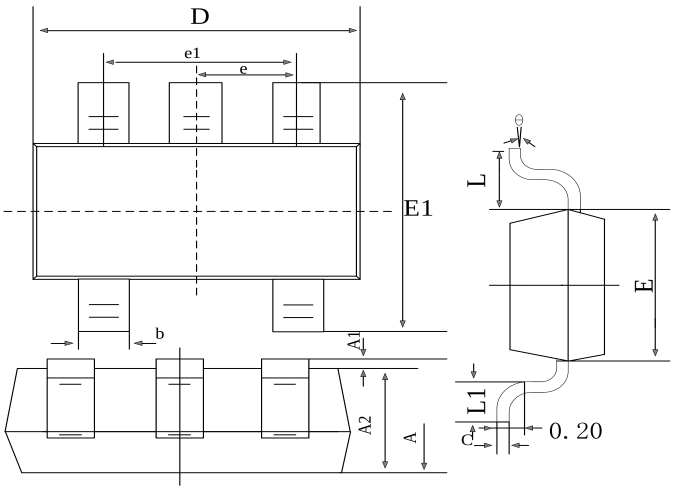
Package Type: SOT-89-3L (J1)



SOT-89-3L (J1)		
Dimension	Min.	Max.
A2	1.40	1.60
a	0.45	0.55
b	0.38	0.48
c	0.36	0.46
D	4.40	4.60
D1	1.60	1.80
E	2.40	2.60
E1	4.00	4.30
e	1.00	2.00
e1	2.95	3.05
L1	0.80	1.00
L2	0.65	0.75
All measurements in "mm"		

Package Outline (All measurements in mm)

Package Type: SOT-23-5L (J1)



SOT-23-5L (J1)		
Dimension	Min.	Max.
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.85	3.05
E	1.50	1.70
E1	2.65	2.95
e	0.95 (BSC)	
e1	1.80	2.00
L	0.30	0.60
Θ	0°	8°
All measurements in "mm"		

Disclaimer

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